| REV | DESCRIPTION | DATE | PREP | APPD |
|---|---|---|---|---|
| C | CO-15263 | 7/15/09 | SM | HW |

| | | DATE |
|---|---|---|
| PREPARED BY | S. Murphy | 6/19/08 |
| QUALITY | R. Smith | 6/19/08 |
| ENGINEERING | H. Wilson | 6/19/08 |
| | | |
| | | |

VECTRON INTERNATIONAL
MOUNT HOLLY SPRINGS, PA 17065

# Specification, Hybrid TCXO

Hi-Rel Standard

| CODE IDENT NO | SIZE | DWG. NO. | REV |
|---|---|---|---|
| 00136 | A | DOC200103 | C |

UNSPECIFIED TOLERANCES: N/A

## 1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid TCXOs produced by Vectron International. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC200103 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military, Ruggedized COTS or Commercial environments.

## 2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

| | |
|---|---|
| MIL-PRF-55310 | Oscillators, Crystal Controlled, General Specification For |
| MIL-PRF-38534 | Hybrid Microcircuits, General Specification For |

Standards

| | |
|---|---|
| MIL-STD-202 | Test Method Standard, Electronic and Electrical Component Parts |
| MIL-STD-883 | Test Methods and Procedures for Microelectronics |
| MIL-STD-1686 | Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment |

Vectron International

| | |
|---|---|
| HT-67849 | Test Specification, OS-68338 Hybrids, Hi-Rel Standard |
| QSP-90100 | Quality Systems Manual, Vectron International |
| VL-65339 | Identification Common Documents, Materials and Processes, Hi-Rel XO |

## 3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310. Primarily developed as a Class S specification, options are imbedded within it to also produce Class B, Engineering Model and Commercial Model devices. Devices carry a Class 2 ESDS classification.

3.2 Item Identification. External packaging choices are either metal flatpacks or DDIP with either Sinewave or CMOS logic output. Unique Model Number Series' are utilized to identify device package configurations and output waveform as listed in Table 1.

3.3 Absolute Maximum Ratings.

| | |
|---|---|
| a. Supply Voltage Range ($V_{CC}$): | -0.5Vdc to +7.0Vdc (CMOS) |
| b. Storage Temperature Range ($T_{STG}$): | -65°C to +125°C |
| c. Junction Temperature ($T_J$): | +175°C |
| d. Lead Temperature (soldering, 10 seconds): | +300°C |
| e. Output Source/Sink Current | ±50 mA |

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs utilize a 4-point crystal mount. When Class S is specified, a radiation tolerance of 100krad (Si) (RHA level R) is included without altering the device's internal topography. For all Class S and Class B products, components meet the Element Evaluation requirements of MIL-PRF-55310, Appendix B. If Design Pedigree Code "E" is chosen, Enhanced Element Evaluation per Appendix A will be performed.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms)
Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on radiation hardened part numbers to further verify lot pedigree. Traceability of all components and production lots are

in accordance with MIL-PRF-38534, as a minimum. Tabulated records are provided as a part of the deliverable data package. Devices are handled in accordance with MIL-STD-1686 for Class 1 devices.

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 derived, System of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 4 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree "D" devices (see ¶ 5.2) use the same robust designs found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in paragraphs 3.4.3 and 4.1.

## 4. DETAIL REQUIREMENTS

### 4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. Premium Q swept quartz is standard for all Class S level products because of its superior radiation tolerance. For Class B level products, swept quartz is optional, as required by the customer. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

4.1.2 Passive Components. Where possible, Established Reliability (ER) failure level R and S passive components are employed. Otherwise, all components comply with the Element Evaluation requirements of MIL-PRF-55310, Appendix B.

4.1.3 Class S Microcircuits. Microcircuits are procured from wafer lots that have passed MIL-PRF-55310 Lot Acceptance Tests for Class S devices. The prescribed die carries a Class 2 ESDS classification in accordance with MIL-PRF-38535. Although radiation testing is not performed at the oscillator level, Design Pedigree Codes E and R versions of this TCXO are acceptable for use in environments of up to 100 krads total dose by analysis of the individual components. Sinewave devices are assembled with all bipolar semiconductors. ACMOS devices are assembled with all bipolar semiconductors with the exception of the ACMOS chip used to provide the CMOS output. An ACMOS die from a radiation tested and certified wafer lot will be provided for all Class S versions of this TCXO. This microcircuit is certified for 100krad(Si) total ionizing dose (TID), RHA level R (2X minimum margin). NSC, as the 54ACT designer, rates the SEU LET at >40 MeV and SEL at >120MeV for the FACT™ family (AN-932). Our wafer testing does not include these parameters and determinations, but

by design similarity. A copy of the parts list and materials can be provided for customer review upon request.

4.1.3.1 Class B Microcircuits. When specified, microcircuits assembled into Pedigree Codes B and C devices (¶ 5.2a) are procured from wafer lots that have passed MIL-PRF-55310 element evaluations for Class B devices.

4.1.4 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. Package lots are upscreened in accordance with the requirements of MIL-PRF-38534 as applicable.

4.1.5 Traceability. Class S active device lots are homogenous and traceable to the manufacturer's individual wafer. Swept Quartz Crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable. All other elements and materials are traceable to their incoming inspection lots. Manufacturing lot and date code information shall be recorded, by TCXO serial number, of every component and all materials used in the manufacture of that TCXO. All semiconductors used in the manufacture of a given production lot of TCXOs shall be from the same wafer and have the same manufacturing lot date code. A production lot, as defined by Vectron, is all oscillators that have been kitted and assembled as a single group. After the initial kitting and assembly, this production lot may be divided into multiple sublots to facilitate alignment and test capacity and may be sealed at multiple times within a 13 week window.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.

4.2.2 Thermal Characteristics. Because these TCXOs are multichip hybrid designs, the actual $\theta_{jc}$ to any one given semiconductor die will vary, but the combined average for all active devices results in a $\theta_{jc}$ of approximately 40°C/W. The typical die temperature rise at any one given semiconductor is 2°C to 4°C. With the oscillator operating at +125°C, the average junction temperature is approximately +129°C and under no circumstance will it ever exceed the maximum manufacturer's rated junction temperature of +150°C.

4.3 Electrical.

4.3.1 Input Power. CMOS devices are designed for 3.3 or 5.0 volt dc operation, ±5%. Sinewave devices are designed for 5.0, 12.0 or 15.0 volt dc operation, ±5%.

4.3.2 Temperature Range. Operating range is IAW the chosen temperature stability code.

4.3.3 Frequency Tolerance. Temperature stability includes initial accuracy at +25°C (with EFC), load ±10% and supply ±5%. All devices include an EFC pin and the external frequency

adjustment shall be accomplished by connecting a resistor or trimmer potentiometer from it to GND. The resistance range is 0Ω or GND to 20KΩ max. Nominal frequency typically occurs in the range of 7.5KΩ to 12.5KΩ.

4.3.4 Frequency Aging. Aging limits, when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1 ppm for the first year and ±5 ppm for 10 years for oscillators that use crystals in the 10 MHz to 75 MHz range. For oscillators that use crystals greater than 75 MHz, the aging shall not exceed ±2 ppm for the first year and ±10 ppm for 10 years.

4.3.4.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-Day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time. Vectron's automated aging systems acquire data every four hours, compared to the minimum MIL-PRF-55310 requirement of once every 72 hours. This makes an extensive amount of data available to perform very accurate aging projections. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to the full 30 Day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.5 Operating Characteristics. See Tables 2 and 3. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10 msec typical and 30 msec maximum.

4.3.6 Output Load. Standard Sinewave (50 ohms) and CMOS (10kΩ, 15pF) test loads are in accordance with MIL-PRF-55310.

4.3.7 Phase Noise. Contact factory for typical performance. If custom and/or guaranteed performance is required, Vectron can assign a custom part number.

## 5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 16$^{th}$ character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A Testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

**(S)** MIL-PRF-55310 Class S Screening, Groups A & B QCI
**(C)** Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
**(B)** MIL-PRF-55310 Class B Screening, Groups A & B QCI

**(X)** Engineering Model (EM)
**(Z)** Commercial Model (CM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be selected or added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):
**(E)** Class S components, Enhanced Element Evaluation, Swept Quartz
**(R)** Class S components, Swept Quartz
**(B)** Class B components, Swept Quartz
**(C)** Class B components, Cultured Quartz
**(D)** COTS components, Cultured Quartz
b. Input Voltage as the 15th character
c. Frequency-Temperature Slew Test
d. Radiographic Inspection
e. Group C Inspection: MIL-PRF-55310 (requires 8 pc. sample)
f. Group C Inspection: MIL-PRF-38534 (requires 8 pc. sample – 5 pc. Life, 3 pc. RGA)
g. Internal Water-Vapor Content (RGA) samples and test performance
h. MTBF Reliability Calculations
i. Worst Case/Derating Analysis
j. Deliverable Process Identification Documentation (PID)
k. Customer Source Inspection (pre-cap / final)

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices:

a. Completed assembly and screening lot travelers, including rework history.
b. Electrical test variables data, identified by unique serial number.
c. Frequency-Temperature Slew plots, Radiographic data, Group C data and RGA data as required by purchase order.

5.5 Discrepant Material. All MRB authority resides with the procuring activity.

5.6 Failure Analysis. Any catastrophic failure (no output, no input current) at Post Burn-In or after will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

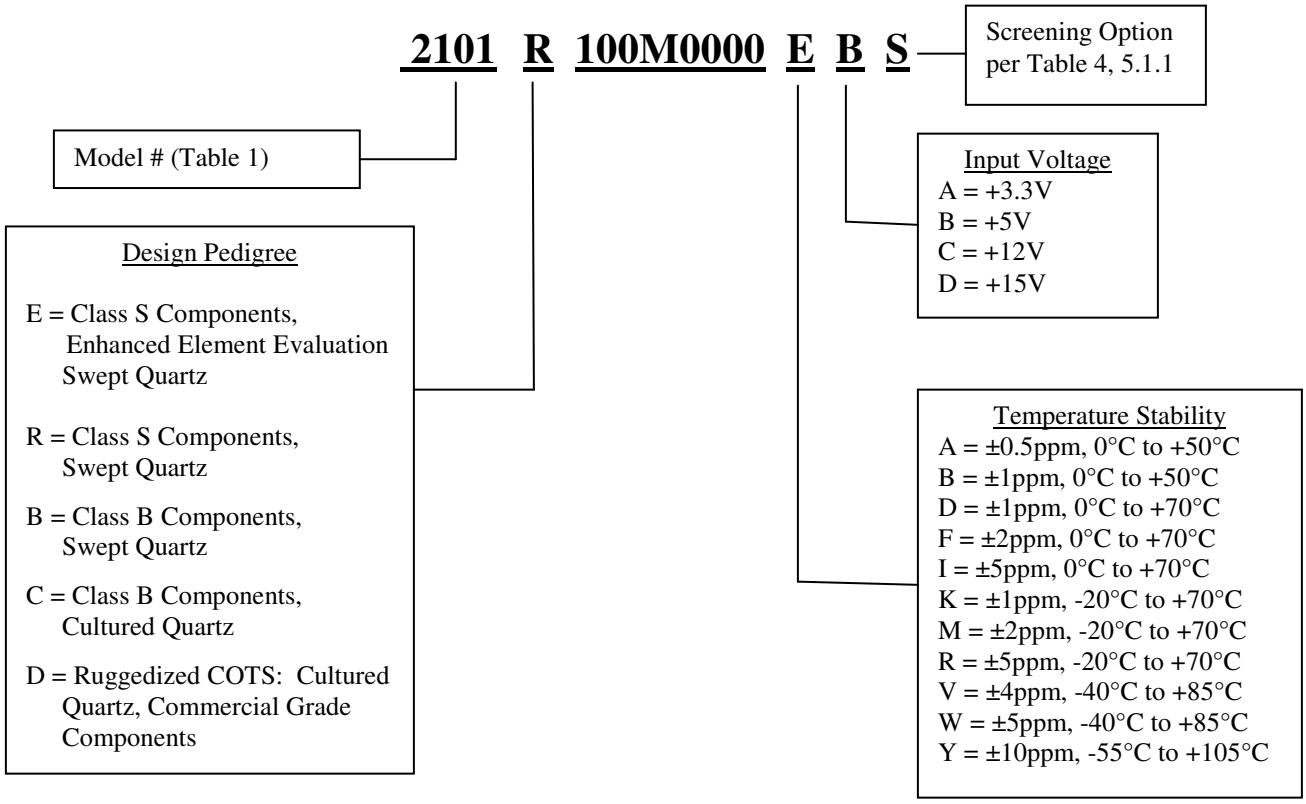
## 6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with MIL-STD-1686 for Class 1 devices.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 16 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:




7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S designs correspond to letters “E” and “R” and are described in paragraph 5.2a. Class B variants correspond to either letter “B” or “C” and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, correspond to letter “D”.

7.1.2.1 Input Voltage. Voltage is the 15th character. Voltage availability is dependant on platform.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Screening Options. The 16th character is the Screening Option selected from Table 4.

7.2 Optional Design, Test and Data Parameters. Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru k).

1/. All unassigned pins have no internal connections or ties.

| HI-REL STANDARD MODEL # | PACKAGE | OUTPUT | PIN I/O 1/ | | | | MECHANICAL OUTLINE |
|---|---|---|---|---|---|---|---|
| | | | Vcc | Out | Gnd/Case | EFC | |
| 2101 | 24 Pin DDIP | CMOS | 24 | 13 | 12 | 1 | FIGURE 1 |
| 2102 | 32 Lead Flatpack | CMOS | 11, 13 | 12 | 5 | 4 | FIGURE 2 |
| 2103 | 24 Lead Flatpack | CMOS | 24 | 13 | 12 | 1 | FIGURE 3 |
| 2104 | 14 Lead Flatpack | CMOS | 2 | 13 | 1, 3, 7, 12, 14 | 6 | FIGURE 4 |
| 2111 | 24 Pin DDIP | Sine | 24 | 13 | 12 | 1 | FIGURE 1 |
| 2112 | 32 Lead Flatpack | Sine | 11, 13 | 12 | 5 | 4 | FIGURE 2 |
| 2113 | 24 Lead Flatpack | Sine | 24 | 13 | 12 | 1 | FIGURE 3 |
| 2114 | 14 Lead Flatpack | Sine | 2 | 13 | 7, 14 | 6 | FIGURE 4 |

**TABLE 1 -** Item Identification and Package Outline

| **Models 2101, 2102, 2103, 2104** | | | | | | |
|---|---|---|---|---|---|---|
| Supply Voltage Options1/: +3.3V or +5V | | | | | | |
| Frequency Range (MHz) | Current (mA) (max, no load) 5.25V | 3.465V | Rise / Fall Times (ns max.)2/ | Duty Cycle (%) | Max CMOS Loads 5.25V | 3.465V |
| 0.300 - 100 | 50 | 35 | 5 | 40 to 60 | 10 | 5 |

1/. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310.
2/. Tested with 2 CMOS loads.

**TABLE 2 -** Electrical Performance Characteristics

| **Model 2111** | | | | | | |
|---|---|---|---|---|---|---|
| Supply Voltage Options: +5V, +12V or +15V | | | | | | |
| Frequency Range (MHz) | Current (mA) (max, no load) 5V | 12V/15V | Min Power Out (dBm) 5V | 12V/15V | Harmonics/ Subharmonics (>75MHz) (dBc) | Spurious (dBc) |
| 10 - 225 | 20 | 35 | +3 | +7 | <-20 | <-70 |

**TABLE 2A -** Electrical Performance Characteristics

| **Models 2112, 2114** | | | | | | |
|---|---|---|---|---|---|---|
| Supply Voltage Options: +5V, +12V or +15V | | | | | | |
| Frequency Range (MHz) | Current (mA) (max, no load) 5V | 12V/15V | Min Power Out (dBm) 5V | 12V/15V | Harmonics/ Subharmonics (>75MHz) (dBc) | Spurious (dBc) |
| 10 - 150 | 20 | 35 | +3 | +7 | <-20 | <-70 |

**TABLE 2B -** Electrical Performance Characteristics

| **Model 2113** | | | | | | |
|---|---|---|---|---|---|---|
| Supply Voltage Options: +12V or +15V | | | | | | |
| Frequency Range (MHz) | Current (mA) (max, no load) 12V | 15V | Min Power Out (dBm) 12V | 15V | Harmonics/ Subharmonics (>75MHz) (dBc) | Spurious (dBc) |
| 10 - 425 | 25 | 35 | +5 | +7 | <-20 | <-70 |

**TABLE 2C -** Electrical Performance Characteristics

| OPERATION LISTING | REQUIREMENTS AND CONDITIONS | VECTRON TEST PROCEDURE |
|---|---|---|
| | | |
| @ all Electrical tests | | |
| Input Current (no load) | MIL-PRF-55310, Para 4.8.5.1 | GR-51681 |
| Initial Accuracy @ Ref. Temp. | MIL-PRF-55310, Para 4.8.6 | GR-51596 |
| Output Logic Voltage Levels | MIL-PRF-55310, Para 4.8.21.3 | GR-51597 |
| Rise and Fall Times | MIL-PRF-55310, Para 4.8.22 | GR-51599 |
| Duty Cycle | MIL-PRF-55310, Para 4.8.23 | GR-51601 |
| | | |
| @ Post Burn-In Electrical only | | |
| Overvoltage Survivability | MIL-PRF-55310, Para 4.8.4 | GR-37269 |
| Initial Freq. – Temp. Accuracy | MIL-PRF-55310, Para 4.8.10.1 | GR-51602 |
| Freq. – Voltage Tolerance | MIL-PRF-55310, Para 4.8.14 | GR-51602 |
| Start-up Time (fast/slow start) | MIL-PRF-55310, Para 4.8.29 | GR-61352 |
| | | |

**TABLE 3** - Electrical Test Parameters

**SCREENING & TESTING OPTIONS**

| Option Code | S | C | B | X | Z |
|---|---|---|---|---|---|
| **Screening** (By Class Similarity) | Mil-PRF-55310 Class 'S' | Mil-PRF-55310 Class 'B' modified | Mil-PRF-55310 Class 'B' | Engineering Model (EM) | Commercial Model (CM) |
| Non-Destruct Wire Bond Pull | 100% | N/A | N/A | N/A | N/A |
| Internal Visual | M883, Method 2017 for Class 'S' | M883, Method 2017 for Class 'B' | M883, Method 2017 for Class 'B' | M883, Method 2017 for Class 'B' | AQL Sample |
| Stabilization Bake | 48 hrs min @ +150°C | 48 hrs min @ +150°C | 48 hrs min @ +150°C | 24 hrs min @ +150°C | 24 hrs min @ +150°C |
| Thermal Shock | M883, Method 1011, TC 'A' | N/A | N/A | N/A | N/A |
| Temperature Cycling | M883, Method 1010, TC 'B' | M883, Method 1010, TC 'B' | M883, Method 1010, TC 'B' | N/A | N/A |
| Constant Acceleration | M883, Method 2001, TC 'A' (5000 g, Y1 Axis only) | M883, Method 2001, TC 'A' (5000 g, Y1 Axis only) | M883, Method 2001, TC 'A' (5000 g, Y1 Axis only) | N/A | N/A |
| Seal Test (fine & gross) | 100% | 100% | 100% | 100% | AQL Sample |
| PIND | M883, Method 2020, TC 'B' | M883, Method 2020, TC 'B' | N/A | N/A | N/A |
| Electrical Test Frequency, Output levels, Input Current | @ +25°C only | @ +25°C only | @ +25°C only | @ +25°C only | @ +25°C only |
| Burn-In (Powered with load) | +125°C for 240 hours | +125°C for 160 hours | +125°C for 160 hours | N/A | N/A |
| Electrical Test Frequency, Output levels, Input Current | @ +25°C & Temp Extremes | @ +25°C & Temp Extremes | @ +25°C & Temp Extremes | N/A | N/A |
| PDA | 2% applies to Input Current @ +25°C | 10% applies to Input Current @ +25°C | 10% applies to Input Current @ +25°C | N/A | N/A |
| Radiographic | M883, Method 2012 | N/A | N/A | N/A | N/A |
| **Group 'A' Inspection** | 100% | Sample per Mil-PRF-55310 | Sample per Mil-PRF-55310 | N/A | N/A |
| **Group 'B' Inspection** (30 day Aging @ +70°C) | 100% | Sample per Mil-PRF-55310 | Sample per Mil-PRF-55310 | N/A | N/A |

**TABLE 4** - Screening & Test Matrix

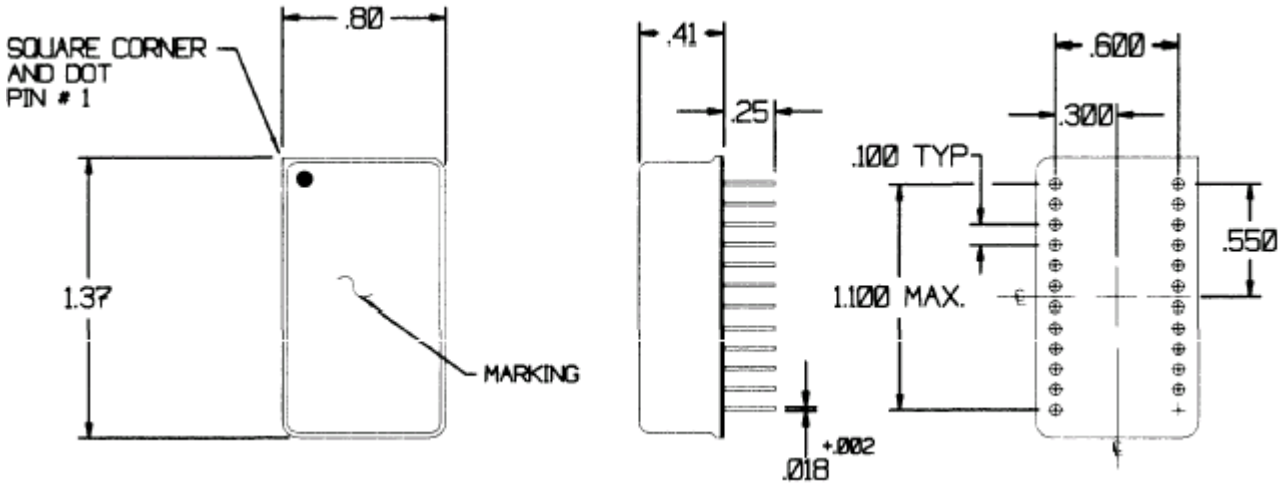



**FIGURE 1**
Models 2101 & 2111 Package Outline
Replaces Vectron Legacy Models 566, 567, 929 and 930

| SIZE | CODE IDENT NO. | THIRD ANGLE PROJECTION | UNSPECIFIED TOLERANCES | DWG NO. | REV. | SHEET |
|---|---|---|---|---|---|---|
| **A** | **00136** | | **N/A** | **DOC200103** | **C** | **13** |

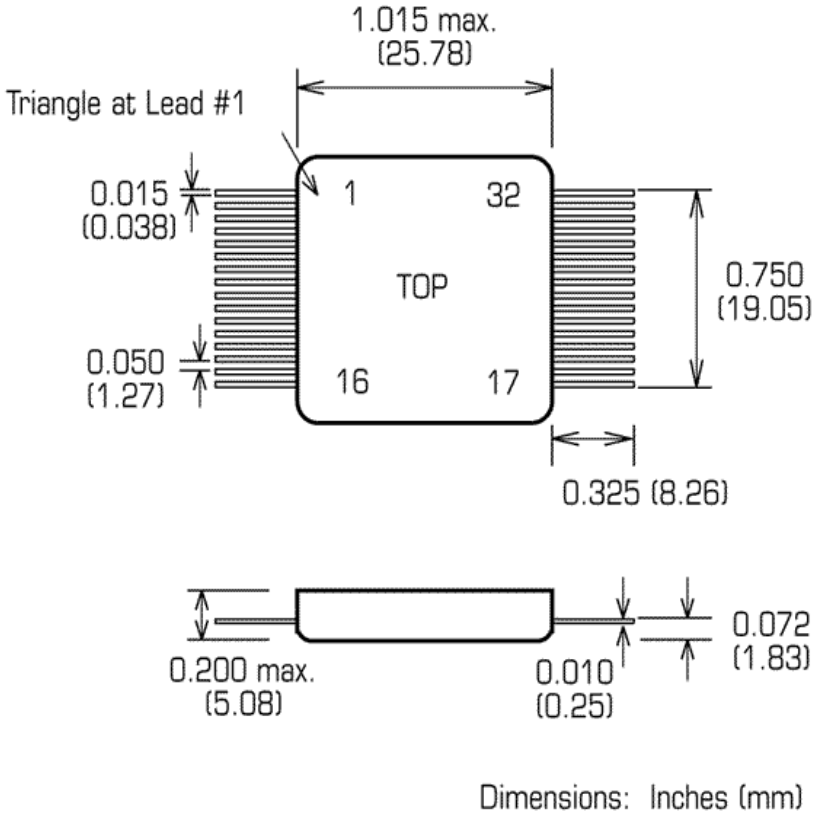



**FIGURE 2**
Models 2102 & 2112 Package Outline
Replaces Vectron Legacy Models 623 and 1623

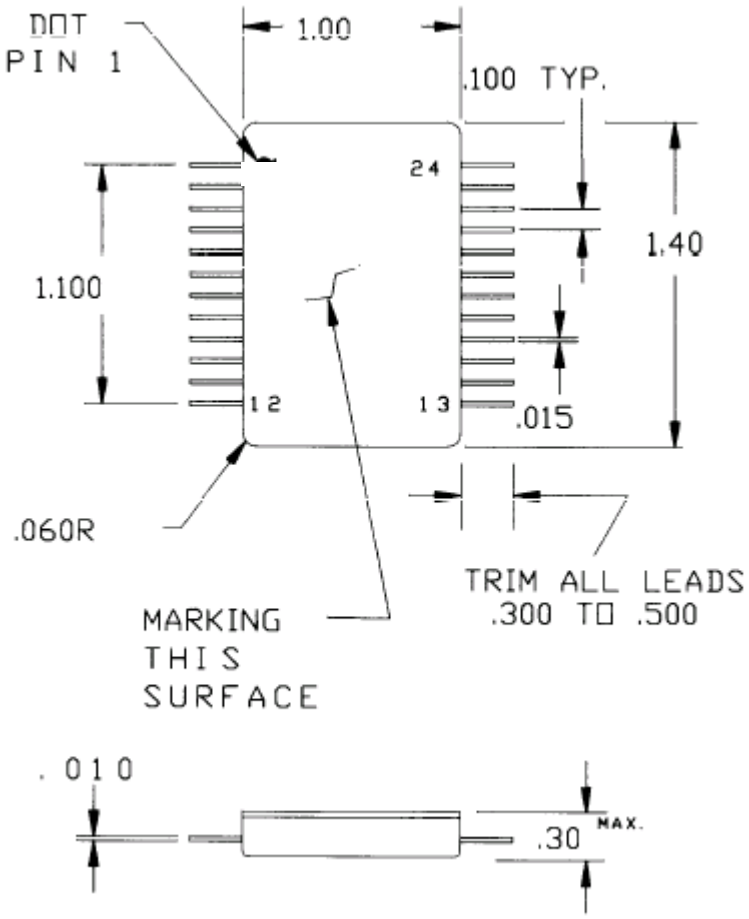



**FIGURE 3**
Models 2103 & 2113 Package Outline
Replaces Vectron Legacy Model 568

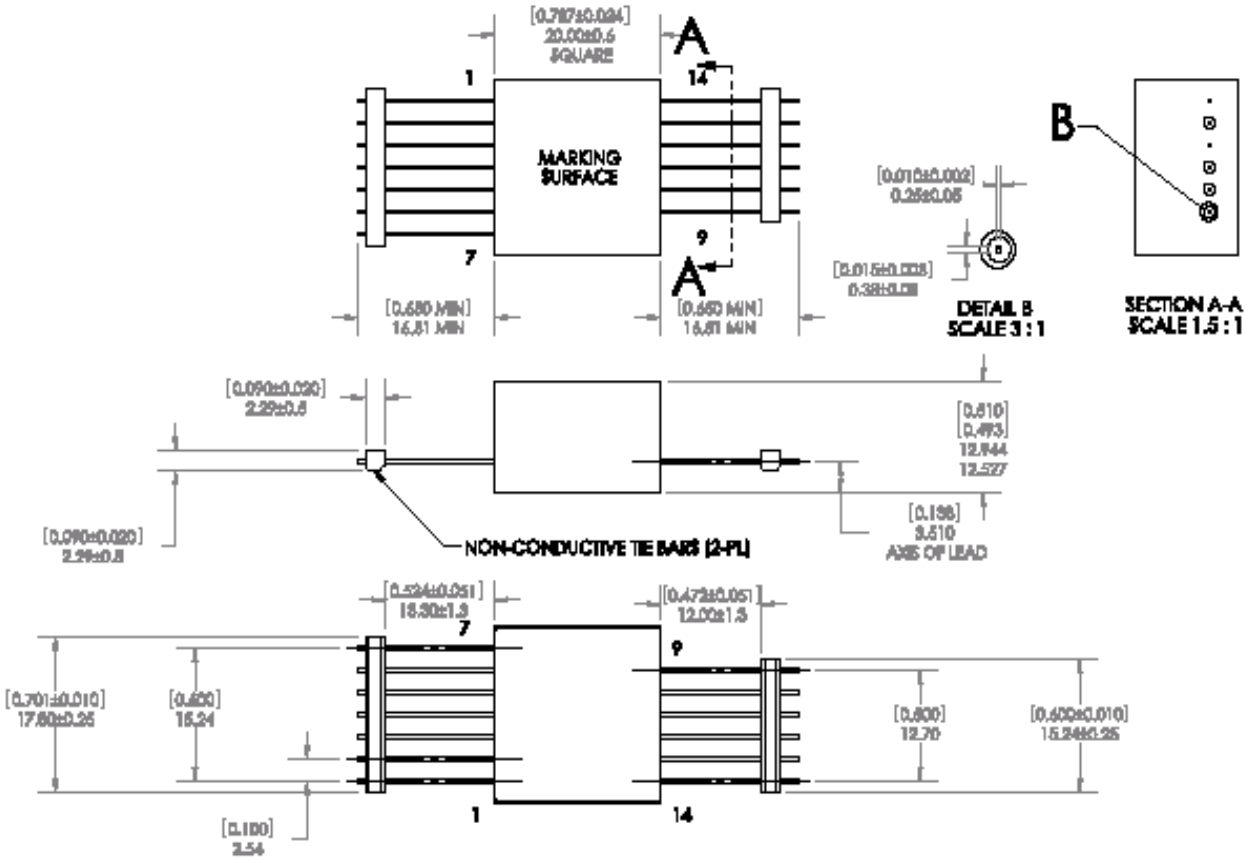



**FIGURE 4**
Models 2104 & 2114 Package Outline
Replaces Vectron Legacy Model 2501

| SIZE | CODE IDENT NO. | THIRD ANGLE PROJECTION | UNSPECIFIED TOLERANCES | DWG NO. | REV. | SHEET |
|---|---|---|---|---|---|---|
| **A** | **00136** | | **N/A** | **DOC200103** | **C** | **16** |

# Appendix A

## ENHANCED ELEMENT EVALUATION

(Sheets 18 through 20)

## MICROCIRCUIT ENHANCED ELEMENT EVALUATION

| Subgroup | Class K | Test | Mil-STD-883 Method | Mil-STD-883 Condition | Quantity (accept number) | Mil-PRF-38534 Reference Paragraph |
|---|---|---|---|---|---|---|
| 1 | X | Element Electrical<br>A. May perform at wafer level<br>B. All failures shall be removed from the lot<br>C. Perform at room ambient | | | 100% | C.3.3.1 |
| 2 | X | Element Visual | 2010 | | 100% | C.3.3.2 |
| 3 | X | Internal Visual | 2010 | | 10(0) or 22(0)<br>(See Notes 1 & 2) | C.3.3.3<br>C.3.3.4.2 |
| 4 | X | Temperature Cycling | 1010 | C | 10(0)<br>22(0)<br>(See Notes 1 & 2) | C.3.3.3 |
| | X | Mechanical Shock<br>or<br>Constant Acceleration | 2002<br><br>2001 | B, Y1 direction<br>3,000 G, Y1 direction | | |
| | X | Interim Electrical | | | | C.3.3.4.3 |
| | X | Burn-In | 1015 | 240 hours minimum at +125°C | | |
| | X | Post Burn-In Electrical | | | | C.3.3.4.3 |
| | X | Steady State Life | 1005 | | | |
| | X | Final Electrical | | | | C.3.3.4.3 |
| 5 | X | Wire Bond Evaluation | 2011 | | 10(0) wires or<br>20(1) wires | C.3.3.3<br>C.3.3.5 |
| 6 | X | SEM | 2018 | | See method 2018<br>& Note 2 | C.3.3.6 |

NOTES:

1. Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.
2. Subgroups 3, 4 & 5 shall be performed in the order listed in Table 1. Subgroup 6 may be performed at any time.

## SEMICONDUCTOR ENHANCED ELEMENT EVALUATION

| Subgroup | Class K | Test | Mil-STD-750 | | Quantity (accept number) | Mil-PRF-38534 Reference Paragraph |
|---|---|---|---|---|---|---|
| | | | Method | Condition | | |
| 1 | X | Element Electrical<br>A. May perform at wafer level<br>B. All failures shall be removed from the lot | | Perform at room ambient | 100% | C.3.3.1 |
| 2 | X | Element Visual | 2069, 2070, 2072, 2073 | | 100% | C.3.3.2 |
| 3 | X | Internal Visual | 2069, 2070, 2072, 2073, 2074 | | 10(0) or 22(0) (Notes 1 & 2) | C.3.3.3<br>C.3.3.4.2 |
| 4 | X | Temperature Cycling | 1051 | C | 10(0)<br>22(0)<br>(See Notes 1 & 2) | C.3.3.3 |
| | X | Surge Current (when applicable) | 4066 | A or B as specified | | |
| | X | Constant Acceleration | 2006<br>2001 | Y1 direction 20,000 G / 10,000 G for Pd ≥ 10W | | |
| | X | Interim Electrical | | | | C.3.3.4.3 |
| | X | High Temperature Reverse Bias (HTRB) | 1039<br>1042<br>1038 | A<br>B<br>A | | |
| | X | Interim Electrical & Delta | | Complete Within 16 hrs of HTRB completion | | |
| | X | Burn-In 240 hours | 1039, 1042<br>1038<br>1040 | B<br>A<br>B | | |
| | X | Post Burn-In Electrical | | | | C.3.3.4.3 |
| | X | Steady State Life 1000 hours | 1026<br>1037<br>1042<br>1048 | | | |
| | X | Final Electrical | | | | C.3.3.4.3 |
| 5 | X | Wire Bond Evaluation | 2011 | | 10(0) wires or 20(1) wires | C.3.3.3<br>C.3.3.5 |
| 6 | X | SEM | 2018<br>2077 | | See method 2018 or 2077 & Note 2 | C.3.3.6 |

NOTES:

1. Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.
2. Subgroups 3, 4 & 5 shall be performed in the order listed in Table 1. Subgroup 6 may be performed at any time.

## PASSIVE COMPONENTS ENHANCED ELEMENT EVALUATION

| Part Type | Test | Requirements Paragraph | Sample Size | Allowable Rejects |
|---|---|---|---|---|
| **Ceramic capacitors** (Production lot definition shall be per M55681 or M123 for chips, or M49470 T-level for stacks) | | | | |
| M55681 FRL S or M123 (chips) | N/A | N/A | N/A | N/A |
| DSCC Dwg COTS (chips) | Ultrasonic scan or CSAM | M123 | 100% | N/A |
| | Group A | M123 | M123 | M123 |
| | Group B, Subgroups 1 & 2 | M123 | M123 | M123 |
| T-level M49470 (stacked) | N/A | N/A | N/A | N/A |
| General purpose M49470, DSCC dwg or COTS (stacked) | Ultrasonic scan or CSAM | M49470 for T-level | 100% | N/A |
| | Group A | M49470 for T-level | M49470 for T-level | M49470 for T-level |
| | Group B, Subgroups 2, 4 & 5b | M49470 for T-level | M49470 for T-level | M49470 for T-level |
| **Tantalum Chip Capacitors** (Note: Stacking tantalum chips will require a repeat of the entire Group A in M55365 with minimum Weibull C and surge current option C. Production lot definition shall be per M55365.) | | | | |
| M55365 | Group A (Weibull C minimum with surge current option C) | M55365 | M55365 | M55365 |
| DSCC Dwg, COTS | Group A (Weibull C minimum with surge current option C) | M55365 | M55365 | M55365 |
| | Group B | M55365 | M55365 | M55365 |
| **Resistor Chips** (Note: Gluing one resistor chip on top of another to change a design or save on real estate is not allowable without extensive design/process verification, long term testing, and hybrid re-qualification. Production lot definition shall be per M55342). | | | | |
| M55342 FRL R or S | N/A | N/A | N/A | N/A |
| DSCC Dwg, COTS | Group A | M55342 for T-level | M55342 for T-level | M55342 for T-level |
| | Group B | M55342 for T-level | M55342 for T-level | M55342 for T-level |
| **Magnetics** (transformers, inductors, coils) (Note: Stacking magnetics will require a repeat of the thermal cycling plus electrical measurements as specified in Group A of Mil-STD-981. Design, workmanship and materials/processes shall conform to Mil-STD-981 requirements. | | | | |
| Custom | Group A | Mil-STD-981 | Mil-STD-981 | Mil-STD-981 |
| | Group B | Mil-STD-981 | Mil-STD-981 | Mil-STD-981 |